

Application No. : 09/801,241
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IN THE SPECIFICATION

1. On page 5, line 23 through page 6, line 2 of the specification as filed, please amend the text as follows:

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-- In a sixth aspect of the invention, an improved method of designing an integrated circuit device having an extensible processor core, secondary processor (e.g., DSP) or macro function, and memory interface is disclosed. In one embodiment, the method comprises providing an extensible core; providing at least one macro function; providing at least one memory interface; adding an HDL (hardware description language) "wrapper" around the DSP or macro function, the HDL wrapper adapted to (i) translate signals, (ii) buffer memory interfaces, and (iii) synchronize clock signals with the memory interface. In another embodiment, the method comprises providing an extensible core; providing at least one "soft" macro function; providing at least one memory interface as described previously herein; and adapting the "soft" macro function implementation to meet the specification associated with the memory interface.--